REMARKS

The present Amendment amends claim 15, and leaves claims 2-14 unchanged. Therefore, the present application has pending claims 2-15.

Allowed Claims

In the Notice of Allowance mailed on August 25, 2006, the Examiner allowed claims 2-15. However, Applicants discovered an error in claim 15 and submit this Amendment to correct that error. The amendments to claim 15 are fully supported by the disclosure as shown, for example, in Fig. 4 (items 23, 23A-1 to 23A-n, and 23B-1 to 23B-n) and the accompanying text.

Claim 15

The present invention, as described in claim 15, provides a packet communication apparatus, which includes a switch unit, a plurality of ingress interfaces, and a plurality of egress interfaces. The switch unit includes a scheduler for scheduling packet transfer between a plurality of input ports and a plurality of output ports, and further includes a plurality of ingress buffers, each connected to one of the input ports. The ingress interfaces are each connected to one of the ingress buffers and selectively transfers packets received from an input line to the ingress buffer. The egress interfaces are each connected to one of the output ports, and transmits packets received from the switch unit to an output line. In the apparatus of the present invention, each of the ingress interfaces includes plural pairs of storage units including a queue buffer for storing packet data and a register configured to retransmit stored packet data, and each of the ingress interfaces further includes a buffer control unit for selecting one of the pairs to output stored

packet data. The register of the selected pair stores a first data block including header information of a packet received from one of the input lines and routing information for specifying one of the output ports. The queue buffer of the selected pair stores the remaining portion of the received packet. Also in the present apparatus of the present invention, said buffer control unit controls the selected register to output the first data block to one of the ingress buffers. In addition, the scheduler issues an acknowledge signal to the buffer control unit if a path toward the output port specified with the routing information of the first data block in the ingress buffer is available to the ingress buffer. The present invention also includes where the buffer control unit controls the selected queue buffer to output the remaining portion of the received packet to the ingress buffer after receiving the acknowledge signal. Otherwise, the buffer control unit selects one of the other pairs of queue buffer and register to output a new first data block from the register to one of the ingress buffers, thereby replacing the previous first data block with the new first data block in the ingress buffer. The prior art does not disclose all these features.

The above described features of the present invention, as recited in claim 15, are not taught or suggested by any of the references of record. Specifically, the features are not taught or suggested by either Luijten or Chao, whether taken individually or in combination with each other.

Luijten is directed to a switching device and method for controlling the routing of data packets. However, there is no teaching or suggestion in Luijten of the packet communication apparatus as recited in claim 15.

Luijten's switching device includes several input ports and several output ports, where each of the input ports is connectable to a corresponding switch adapter. At least one switch controller controls the routing of incoming data packets from the input ports to the output ports. For each output port, a congestion controller is arranged. In operation, the congestion controller generates grant information, which signals whether the switch adapters are allowed to send the data packet to the output port. For each of the input ports, a data packet access controller marks a data packet as non-compliant if the packet was erroneously sent from the output port.

Features of the present invention, as recited in claim 15, include where each of the ingress interfaces includes plural pairs of storage units including a queue buffer that stores packet data and a register that can retransmit stored packet data, and where each of the ingress interfaces further includes a buffer control unit for selecting one of the pairs to output stored packet data. The register of the selected pair stores a first data block including header information of a packet received from one of the input lines and routing information for specifying one of the output ports. The queue buffer of the selected pair stores the remaining portion of the received packet. Luijten does not disclose each of these features.

For example, Luijten does not teach or suggest where each of the ingress interfaces includes a buffer control unit, as claimed. In the rejection of claim 1 (now canceled), the Examiner asserts that the data packet access controller 40, which is connected to each input port 20 within a switching device 10, corresponds to the scheduler of the present invention. Furthermore, the Examiner asserts that the

control unit 25 corresponds to the buffer control unit of the present invention. However, as described in paragraph 4, lines 30-62, the purpose of the control unit 25 is to lead the data packets that arrive via adapter input lines 50 to output ports 30. the control unit 25 provides the necessary connections between the input ports 20 and the output ports 30, according to the data packet destination information that is contained in each data packet header, and signals to the input buffers 11 when the path for the next data packet in the respective input buffer 11 is free, such that this data packet can be taken from the input buffer 11 and sent to its destination. Based on this description, it is apparent that the control unit 25 corresponds to the scheduler of the present invention, and that Luijten fails to disclose a plurality of buffer control units, where each of the ingress interfaces includes a buffer control unit, in the manner claimed.

Other features of the present invention, as recited in claim 15, include where the scheduler issues an acknowledge signal to the buffer control unit if a path toward the output port specified with the routing information of the first data block in the ingress buffer is available to the ingress buffer. Luijten does not disclose this feature.

Additional features of the present invention, as recited in claim 15, include where the buffer control unit controls the selected queue buffer to output the remaining portion of the received packet to the ingress buffer after receiving the acknowledge signal. Otherwise, the buffer control unit selects one of the other pairs of queue buffer and register to output a new first data block from the register to one

of the ingress buffers to replace the previous first data block with the new first data block in the ingress buffer. This feature is not disclosed in Luijten.

Therefore, Luijten fails to teach or suggest "wherein each of said ingress interfaces includes plural pairs of storage units including a queue buffer for storing packet data and a register capable of retransmitting stored packet data, and wherein each of said ingress interfaces further includes a buffer control unit for selecting one of said pairs to output stored packet data, the register of the selected pair storing a first data block including header information of a packet received from one of said input lines and routing information for specifying one of said output ports, the queue buffer of the selected pair storing the remaining portion of the received packet" as recited in claim15.

Furthermore, Luijten fails to teach or suggest "wherein said scheduler issues an acknowledge signal to the buffer control unit if a path toward the output port specified with the routing information of the first data block in the ingress buffer is available to the ingress buffer" as recited in claim 15.

Even further, Luijten fails to teach or suggest "wherein the buffer control unit controls the selected queue buffer to output the remaining portion of the received packet to the ingress buffer after receiving said acknowledge signal, and otherwise, the buffer control unit selects one of the other pairs of queue buffer and register to output a new first data block from the register to one of said ingress buffers, thereby to replace the previous first data block with the new first data block in the ingress buffer" as recited in claim 15.

The above noted deficiencies of Luijten are not supplied by any of the other references, particularly Chao. Therefore, combining the teachings of Chao with Luijten still fails to teach or suggest the features of the present invention, as now more clearly recited in the claims.

Chao discloses the design and implementation of an abacus switch, or more specifically, a scalable multicast asynchronous transfer mode (ATM) switch. However, there is no teaching or suggestion in Chao of the packet data transfer controlling method as recited in claim 15.

Chao's multicast ATM switch is scalable from a few tens to a few thousands of input ports. The switch, which is called an abacus switch, has a non-blocking switch fabric followed by small switch modules at the output ports. It has buffers at the input and output ports. Cell replication, cell routing, output contention and resolution, and cell addressing are all performed in a distributed way so that it can be scaled up to thousands of input and output ports.

Features of the present invention, as recited in claim 15, include where each of the ingress interfaces includes plural pairs of storage units including a queue buffer that stores packet data and a register that can retransmit stored packet data, and where each of the ingress interfaces further includes a buffer control unit for selecting one of the pairs to output stored packet data. The register of the selected pair stores a first data block including header information of a packet received from one of the input lines and routing information for specifying one of the output ports. The queue buffer of the selected pair stores the remaining portion of the received packet. Chao does not disclose these features. For example, as indicated in the

third paragraph on page 836, Chao discloses a mechanism for retransmitting a cell in a stack state. This feature is quite different from storing packet data and a register capable of retransmission, as claimed.

Other features of the present invention, as recited in claim 15, include where the scheduler issues an acknowledge signal to the buffer control unit if a path toward the output port specified with the routing information of the first data block in the ingress buffer is available to the ingress buffer. Chao does not disclose this feature.

Additional features of the present invention, as recited in claim 15, include where the buffer control unit controls the selected queue buffer to output the remaining portion of the received packet to the ingress buffer after receiving the acknowledge signal. Otherwise, the buffer control unit selects one of the other pairs of queue buffer and register to output a new first data block from the register to one of the ingress buffers to replace the previous first data block with the new first data block in the ingress buffer. Chao does not disclose this feature.

Therefore, Chao fails to teach or suggest "wherein each of said ingress interfaces includes plural pairs of storage units including a queue buffer for storing packet data and a register capable of retransmitting stored packet data, and wherein each of said ingress interfaces further includes a buffer control unit for selecting one of said pairs to output stored packet data, the register of the selected pair storing a first data block including header information of a packet received from one of said input lines and routing information for specifying one of said output ports, the queue buffer of the selected pair storing the remaining portion of the received packet" as recited in claim15.

Furthermore, Chao fails to teach or suggest "wherein said scheduler issues an acknowledge signal to the buffer control unit if a path toward the output port specified with the routing information of the first data block in the ingress buffer is available to the ingress buffer" as recited in claim 15.

Even further, Chao fails to teach or suggest "wherein the buffer control unit controls the selected queue buffer to output the remaining portion of the received packet to the ingress buffer after receiving said acknowledge signal, and otherwise, the buffer control unit selects one of the other pairs of queue buffer and register to output a new first data block from the register to one of said ingress buffers, thereby to replace the previous first data block with the new first data block in the ingress buffer" as recited in claim 15.

Both Luijten and Chao suffer from the same deficiencies relative to the features of the present invention, as recited in claim 15. Therefore, combining the teachings of Luijten and Chao does not render obvious the features of the present invention, as recited in claim 15. Accordingly, reconsideration and withdrawal of the 35 U.S.C. §103(a) rejection of claim 15 as being unpatentable over Luijten in view of Chao are respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references used in the rejection of claim 15.

In view of the foregoing amendments and remarks, Applicants submit that claims 2-15 are in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the Deposit account of Mattingly, Stanger, Malur & Brundidge, P.C., Deposit Account No. 50-1417 (referencing attorney docket no. 520.41245X00).

Respectfully submitted,

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